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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,668	04/30/2001	Radhika Thekkath	MTEC004/00US (0121.00US)	8993

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EXAMINER	
PHAM, CHRYSTINE	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,668	THEKKATH ET AL.	
	Examiner	Art Unit	
	Chrystine Pham	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,13 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,13 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 16th, 2005 has been entered.

2. This action is responsive to Amendment filed on September 16th, 2005. Claims 7-12 and 14-15 have been canceled. Claims 1-4, 6, 13, 16, 19, 20, and 21 have been amended. Claims 1-6, 13, 16-22 are presented for examination.

Response to Amendment

3. In view of the amendment to claim 1 to omit "a trace control register", rejection of claims 1-9 under 35 U.S.C. 112, first paragraph, is hereby withdrawn.

Response to Arguments

4. Applicant's arguments with respect to new limitation "wherein said operating mode is selected from a kernel mode, a supervisor mode, a user mode and a debug mode" recited in independent claims 1, 13, 19-21 have been considered but are moot in view of the new ground(s) of rejection.

5. Other arguments filed September 16th, 2005 have been fully considered but they are not persuasive.

- It should be noted that Applicant has amended the independent claims 1, 13, 19-21 to eliminate references to "**a trace control register**", which was originally claimed as "*includes fields to specify an **operating mode** of said embedded processor, a **current process** being executed by said embedded processor, and **load and store address information***". Instead, Applicant now claims "**specified information**", in place of the "trace control register". In other words, the newly added limitation "specified information" is not required to be a specific "trace control register", however, the "**specified information**" includes the same fields as the originally claimed "**trace control register**", that is to say, the "specified information" also "*includes fields to specify an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information*".
  - As set forth in the final Office Action (pages 2-4), Mann clearly anticipates fields to *specify an **operating mode** of said embedded processor* (see final Office Action, page 3, 1st paragraph; see Man col.5:15-21, *DCSR register, bit field STOP* col.8:28-60), *a **current process** being executed by said embedded processor* (see final Office Action, page 3, last paragraph; see Mann *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60), and ***load and store address** information* (final Office Action, page 4, 1st paragraph; see Mann *read/write operations* col.5:20-37; *trace synchronization entry* col.14:50-53). Thus, it is submitted that the DCSR register (for specifying an **operating mode** of

the embedded processor), the trace synchronization entry (for specifying a **current process** being executed and **load/store address information**) collectively anticipate the "**specified information**".

- Second, Applicant contends, "MANN fails to show or suggest the discrimination of a **current process** within a **multi-tasking** embedded processor" (page 6, 3rd paragraph).
  - However, contrary to Applicant's assertion, in col.15:34-41 and FIG.6F, Mann expressly discloses a trace entry TCODE=1001 as a current task (i.e., **current process**) identifier in a **multi-tasking** operating system. Needless to say, the trace entry TCODE=1001 clearly anticipates a field to specify a current process being executed by a multi-tasking embedded processor.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 13, 16-21 are rejected under 35 U.S.C. 102(3) as being unpatentable over Mann of record (US 6009270, *Mann*) in view of Mann, made of record (US 6314530 B1, *Mann '530*) further in view of Moughani et al., made of record (US 5970246, *Moughani*).

Claim 1

Mann teaches a tracing system (e.g., see FIG.1, FIG.2 & associated text), comprising: a multi-tasking embedded processor (e.g., see *102* FIG.1, FIG.2 & associated text; col.3:65-67; *multi-tasking* col.15:34-41; FIG.6F & associated text), said embedded processor including,

- a processor core for executing instructions (e.g., see *PROCESSOR CORE 104* FIG.1 & associated text; col.4:45-50); and
- trace generation logic (i.e., tracing method) that is operative to periodically generate trace synchronization information (e.g., see *trace synchronization information* Abstract), wherein said trace synchronization information is periodically generated in accordance with specified information (e.g., see *TRACECLK* FIG.2 & associated text; col.7:1-9; see *TRACE CONTROL 218* FIG.2 & associated text; see *TSYNC REGISTER 703* FIG.7 & associated text).
- wherein said specified information includes fields to specify an operating (i.e., debug) mode of said embedded processor (e.g., *DCSR* col.5:15-21; see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67), a current process being executed by said embedded processor (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60), and load and store address

information (see at least *read/write operations, embedded processor device 102, debug registers 210, 206, 218* col.5:20-37; *trace synchronization entry, address* col.14:50-53). Mann does not expressly disclose "wherein said operating mode is selected from a kernel mode, a supervisor mode, and a user mode". However, *Mann '530* discloses a tracing system comprising a multi-tasking embedded processor which includes a processor for executing instructions and trace generation logic operative to generate trace synchronization information in accordance with a specified operating mode, wherein the operating mode is a **kernel mode** (see at least Abstract; *processor core 102* FIG.1 & associated text; *trace control 218* Fig.2 & associated text; *on-chip trace memory, kernel-mode, debugging* col.23:25-33; *privilege level, trace information, trace memory* col.4:30-37; *trace logic, privilege level* col.22:33-45). Furthermore, *Moughani* disclose a trace generation logic that generates trace information in accordance with a specified operating mode, wherein the operating mode is a **supervisor mode** or a **user mode** (see at least *access protect unit 20* FIG.1 & associated text; *trace registers 26* FIG.2 & associated text; *62-80* FIG.6 & associated text; *code tracing, supervisor, user mode* col.2:15-20; *50* FIG.5 & associated text; *Bit field 50, TR, supervisor mode, user mode* col.3:38-67; *decision step 78, trace bit, user mode* col.4:34-65). *Mann '530*, *Moughani* and *Mann* are analogous art because they are directed to generating trace. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Mann '530* and *Moughani* into that of *Mann* for the inclusion of kernel mode, supervisor mode, and user mode. And the motivation for doing so would have been to enable tracing of memory accesses on various levels (i.e., kernel, supervisor, user, or debug modes) without the need

for an emulation system or on-chip emulator. In other words, when the system is operating in kernel, or supervisor modes, tracing is enabled for all areas of the memory, while tracing is limited to certain areas of memory when the system is operating in user mode (see at least *Moughani* Abstract; col.3:3-50-67; col.4:34-52).

Claim 2

The rejection of base claim 1 is incorporated. *Mann* further teaches wherein said specified information enables multiple instances of said periodically generated trace synchronization information (e.g., see *200* FIG.3 & associated text) to be stored at one time (i.e., sent or outputted to) in a trace memory (i.e., trace memory included in said embedded processor) (e.g., see *TRACE CACHE 200* FIG.2 & associated text).

Claim 3

The rejection of base claim 2 is incorporated. Claim recites limitations, which have been addressed in claim 2, therefore, is rejected for the same reasons as cited in claim 2.

Claim 4

The rejection of base claim 2 is incorporated. *Mann* further teaches wherein said multi-tasking embedded processor further includes a trace capture block that receives trace data from said trace generation logic (e.g., see *instruction trace capture* col.4:37-41; see *BRKMODE* TABLE 3 col.8:64-66; see *BRTC* col.6:50-67).

Claim 5

The rejection of base claim 4 is incorporated. *Mann* further teaches wherein said trace capture block sends trace data to an off-chip implementation of said trace memory (e.g., see *HOST SYSTEM H* FIG.1 & associated text; see *200, 230* FIG.3 & associated text).

Claim 6

The rejection of base claim 4 is incorporated. *Mann* further teaches wherein said trace capture block sends trace data to an off-chip implementation of said trace memory (e.g., see *TRACE CACHE 200* FIG.2 & associated text).

Claim 7

The rejection of base claim 6 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 8

The rejection of base claim 7 is incorporated. *Mann* further teaches wherein a first set of said predefined synchronization periods apply to an on-chip implementation of said trace memory (e.g., see *TRACE CACHE 200* FIG.2 & associated text) and a second set of said predetermined synchronization periods apply to an off-chip implementation of said trace memory (e.g., see *200, 230* FIG.3 & associated text).

Claim 9

The rejection of base claim 1 is incorporated. *Mann* further teaches wherein said trace synchronization information includes program counter information (i.e., application space identity information) (e.g., see *COUNTER 701* FIG.7 & associated text; see *current program address* col.16:25-30).

Claim 13

Mann teaches a tracing method, comprising:

Periodically generating trace synchronization information (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60) in accordance with specified information (e.g., see *TRACECLK* FIG.2 & associated text; col.7:1-9), said trace synchronization information including program counter information (e.g., see *COUNTER 701* FIG.7 & associated text; see *current program address* col.16:25-30) and information that enables a determination of a characteristic of an operating (i.e., debug) state (i.e., mode) of a multi-tasking processor (e.g., see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67; *102* FIG.1, FIG.2 & associated text; col.3:65-67; *multi-tasking* col.15:34-41; FIG.6F & associated text); and outputting said trace synchronization information to a trace memory (e.g., see *TRACE CACHE 200* FIG.2 & associated text).

Mann does not expressly disclose "wherein said operating state is selected from a kernel mode, a supervisor mode, and a user mode". However, *Mann '530* discloses a tracing system comprising a multi-tasking embedded processor which includes a processor for executing instructions and trace generation logic operative to generate trace synchronization information in accordance with

a specified operating mode, wherein the operating mode is a **kernel mode** (see at least Abstract; *processor core 102* FIG.1 & associated text; *trace control 218* Fig.2 & associated text; *on-chip trace memory, kernel-mode, debugging* col.23:25-33; *privilege level, trace information, trace memory* col.4:30-37; *trace logic, privilege level* col.22:33-45). Furthermore, *Moughani* disclose a trace generation logic that generates trace information in accordance with a specified operating mode, wherein the operating mode is a **supervisor mode** or a **user mode** (see at least *access protect unit 20* FIG.1 & associated text; *trace registers 26* FIG.2 & associated text; *62-80* FIG.6 & associated text; *code tracing, supervisor, user mode* col.2:15-20; *50* FIG.5 & associated text; *Bit field 50, TR, supervisor mode, user mode* col.3:38-67; *decision step 78, trace bit, user mode* col.4:34-65). *Mann '530, Moughani* and *Mann* are analogous art because they are directed to generating trace. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Mann '530* and *Moughani* into that of *Mann* for the inclusion of kernel mode, supervisor mode, and user mode. And the motivation for doing so would have been to enable tracing of memory accesses on various levels (i.e., kernel, supervisor, user, or debug modes) without the need for an emulation system or on-chip emulator. In other words, when the system is operating in kernel, or supervisor modes, tracing is enabled for all areas of the memory, while tracing is limited to certain areas of memory when the system is operating in user mode (see at least *Moughani* Abstract; col.3:3-50-67; col.4:34-52).

Claims 16-18

Claims recite limitations, which have been addressed in claims 1, 2, 9, therefore, are rejected for the same reasons as cited in claims 1, 2, 9.

Claim 19

Mann teaches a computer program product comprising

- computer-readable program code (i.e., computer data signal) for causing a computer to describe an embedded multi-tasking processor (e.g., see FIG.1 & associated text; see claims 10-11 above; *102* FIG.1, FIG.2 & associated text; col.3:65-67; *multi-tasking* col.15:34-41; FIG.6F & associated text), said embedded processor including a processor core for executing instructions and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with specified information (see claim 1); and
- wherein said specified information includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an operating (i.e., debug) mode of said multi-tasking embedded processor (e.g., see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67), a current process being executed by said embedded processor (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60), and load and store address information (see at least *read/write operations, embedded processor device 102, debug registers 210, 206, 218* col.5:20-37; *trace synchronization entry, address* col.14:50-53); and

- a computer-usable medium (i.e., transmission medium) configured to store the computer-readable program code (e.g., see FIG.2 & associated text).

Mann does not expressly disclose "wherein said operating state is selected from a kernel mode, a supervisor mode, and a user mode". However, *Mann '530* discloses a tracing system comprising a multi-tasking embedded processor which includes a processor for executing instructions and trace generation logic operative to generate trace synchronization information in accordance with a specified operating mode, wherein the operating mode is a **kernel mode** (see at least Abstract; *processor core 102* FIG.1 & associated text; *trace control 218* Fig.2 & associated text; *on-chip trace memory, kernel-mode, debugging* col.23:25-33; *privilege level, trace information, trace memory* col.4:30-37; *trace logic, privilege level* col.22:33-45). Furthermore, *Moughani* disclose a trace generation logic that generates trace information in accordance with a specified operating mode, wherein the operating mode is a **supervisor mode** or a **user mode** (see at least *access protect unit 20* FIG.1 & associated text; *trace registers 26* FIG.2 & associated text; *62-80* FIG.6 & associated text; *code tracing, supervisor, user mode* col.2:15-20; *50* FIG.5 & associated text; *Bit field 50, TR, supervisor mode, user mode* col.3:38-67; *decision step 78, trace bit, user mode* col.4:34-65). *Mann '530, Moughani* and *Mann* are analogous art because they are directed to generating trace. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Mann '530* and *Moughani* into that of *Mann* for the inclusion of kernel mode, supervisor mode, and user mode. And the motivation for doing so would have been to enable tracing of memory accesses on various levels (i.e., kernel, supervisor, user, or debug modes) without the need for an emulation system or on-chip emulator. In other words, when the system is operating in kernel, or supervisor modes, tracing is enabled

for all areas of the memory, while tracing is limited to certain areas of memory when the system is operating in user mode (see at least *Moughani* Abstract; col.3:3-50-67; col.4:34-52).

Claims 20-21

Claims recite limitations, which have been addressed in claims 1, 9, 19, therefore, are rejected for the same reasons as cited in claims 1, 9, 19.

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Mann* in view of *Mann '530* in view of *Moughani* further in view of Shagam of record (US 6311326, *Shagam*).

Claim 22

The rejection of base claim 21 is incorporated. *Mann, Mann '530, and Moughani* (**M3**) do not expressly disclose wherein computer-readable program code is transmitted to said computer over the Internet. However, *Shagam* teaches wherein computer-readable program code (i.e., trace data) is transmitted to said computer over the Internet (e.g., see Abstract; see *400, 402* FIG.3 & associated text; col.1:50-67; col.4:54-56). *Shagam* and *Mann* are analogous art because they are both directed to tracing systems/methods. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Shagam* into that of **M3** for the inclusion of transmitting trace data over the Internet. And the motivation for doing so would have been to facilitate remote online access to and sharing of trace data for debugging software installed on client computers situated in remote locations without

imposing significant performance degradation on the client computer system (e.g., interrupting or impairing the client's ability to do business).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571-272-3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
December 23, 2005

TUAN DAM
SUPERVISORY PATENT EXAMINER